AS5018 Tiny LVCMOS Silicon Oscillator

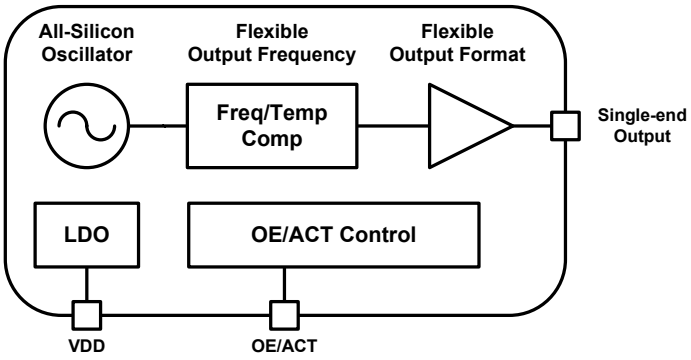
Description

The AS5018 all-silicon oscillator utilizes digital frequency synthesis and sensing technologies to provide a quartz-free, MEMS-free, low jitter clock at any output frequency. The device is factory-programmed to output frequencies ranging from 10 kHz to 125 MHz with 1 Hz resolution and maintains low jitter across its operating range.

There're no mechanical moving parts in the chip, which gives the AS5018 robust immunity to shock and vibration. The AS5018 uses on-chip temperature and strain sensors, and an advanced LC tank architecture to achieve excellent reliability even in high impact shock scenarios.

AS5018's on-chip power supply filtering provides ease of use in noisy systems with switched-mode power supplies.

The AS5018 is factory-configurable for a wide range of output frequencies. Specific configurations are factory programmed at time of shipment, eliminating the long lead times associated with custom oscillators. This process also guarantees 100% electrical testing of every device before shipment.



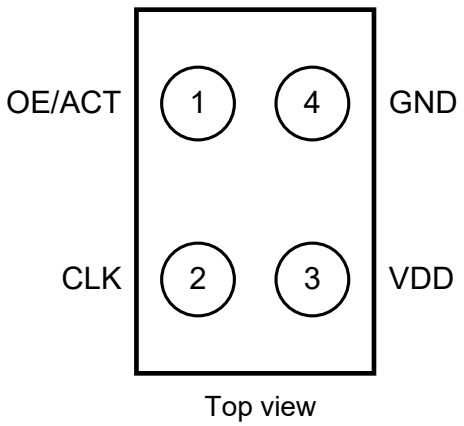
Key Features

- Quartz-free and MEMS-free without mechanical moving parts
- LVCMOS output: 10 kHz to 125 MHz
- Low jitter: 1 ps Typ
  (12 kHz – 20 MHz, @125 MHz)
- Operating temperature range:
  - -40 to 85 ℃ (Industial grade)
  - -40 to 105 ℃ (Extended-Industial grade)
- Frequency tolerance: ±50 ppm (-40 to 105 ℃)
- Immunity to shock and vibration
- Integrated LDO for on-chip power supply noise filtering
- Support 1.8V, 2.5V, 3.3V V_{DD} supply operation
- Tiny package size: 1.2 mm x 1.0 mm

Application

- IoT, Wearable device
- Health and medical monitoring
- Tablet
- Portable audio

Pin definition



Top view

Pin#	Description
1	OE = Output enable. Active high ACT = Device active. Active high
2	CLK = Clock output
3	VDD = Power supply
4	GND = Ground

1. Ordering Guide

XO Series	Description
5018	Fixed Frequency

	Device Type
A	General
X[1]	Factory defined setting

	Device Grade	Temperature Grade
I	Industrial grade	-40 to 85°C
E	Extended industrial grade	-40 to 105°C

5018	A	A	A	-	-	-	-	-	-	-	-	F	B	I	T

	Frequency Range
A	<= 50 MHz
B	> 50 MHz

	Pin#1
A	OE
C	ACT

Device Revision

Frequency Code[2]	Description
Mxxxxxxx	F_{CLK} < 1 MHz
xMxxxxxx	1 MHz <= F_{CLK} < 10 MHz
xxMxxxxx	10 MHz <= F_{CLK} < 100 MHz
xxxMxxxx	100 MHz <= F_{CLK} <= 125 MHz

	Package
F	1210

Code	Packing type	Qty
T	7-inch reel	250
R	13-inch reel	2500
F	13-inch reel	5000
<blank>	ESD bag	Sample

Note:

1. “X” refers to the ID for the unique configuration with factory-defined settings, the value ranges from “B” to “Z”.
2. For example: 125 MHz = 125M0000; 33.33333 MHz = 33M33333.

2. Electrical Specifications

Table 2.1. Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating Temperature Range						
Temperature Range	T_A	-40	–	85	℃	Industrial grade
		-40	–	105	℃	Extended industrial grade
Supply Voltage and Power Consumption						
Supply Voltage	V_{DD}	1.62	–	3.63	V	
Supply Current (F_{CLK} = 25 MHz)	I_{DD}	–	10	11	mA	Tristate Hi-Z (OE = 0)
		–	1	2	mA	Ready State (ACT = 0)
		–	12	14	mA	LVCMOS output (C_L=15pF)
Frequency Range						
Frequency Range	F_{CLK}	0.01	–	125	MHz	LVCMOS output
Frequency Tolerance						
Total frequency tolerance	F_{TOTAL}	-50	–	50	ppm	-40 - 105℃
Notes: Inclusive of initial frequency tolerance at 25℃, temperature stability over the corresponding operation temperature range, 10-year aging at 25℃ and variations over supply voltage, load and humidity after soldering-reflow shift settles.						
IO Characteristics						
Output enable (OE)	V_{IH}	0.7×V_{DD}	–	–	V	Input high voltage
	V_{IL}	–	–	0.3×V_{DD}	V	Input low voltage
	R_{PUP}	–	50	–	kΩ	Internal pull-up resistor to V_{DD}
	T_D	–	–	3	us	Output disable time, F_{CLK} >10 MHz
	T_E	–	–	20	us	Output enable time, F_{CLK} >10 MHz
Device active (ACT)	V_{IH}	0.7×V_{DD}	–	–	V	Input high voltage
	V_{IL}	–	–	0.3×V_{DD}	V	Input low voltage
	R_{PUP}	–	50	–	kΩ	Internal pull-up resistor to V_{DD}
	T_D	–	–	3	us	Output disable time, F_{CLK} >10 MHz
	T_S	–	–	40	us	Device standby time, F_{CLK} >10 MHz
	T_E	–	–	400	us	Device enable time, F_{CLK} >10 MHz
Output Characteristics						
Powerup time	T_{OSC}	–	–	4	ms	Time from power reaches 0.9 × V_{DD} to output frequency (F_{CLK}) within spec
Duty cycle	DC	45	–	55	%	LVCMOS (C_L=15pF)
Rise/Fall time (20% to 80% VPP)	$T_{R/F}$	–	0.5	1.5	ns	LVCMOS (C_L=15pF)
LVCMOS	V_{OH}	0.83×V_{DD}	–	–	V	C_L=15pF
	V_{OL}	–	–	0.17×V_{DD}	V	
Phase Noise and Jitter						
RMS jitter BW: 12k - 20MHz	R_J	–	1	1.5	ps	F_{CLK} >= 100 MHz
		–	1.5	2	ps	F_{CLK} >= 25 MHz
Phase noise 125MHz LVCMOS output V_{DD} = 1.8 - 3.3V	PN_{1k}	–	-73	–	dBc/Hz	Phase noise at 1kHz offset
	PN_{10k}	–	-103	–	dBc/Hz	Phase noise at 10kHz offset
	PN_{100k}	–	-126	–	dBc/Hz	Phase noise at 100kHz offset
	PN_{1M}	–	-141	–	dBc/Hz	Phase noise at 1MHz offset
	PN_{10M}	–	-150	–	dBc/Hz	Phase noise at 10MHz offset

Continued on next page

Parameter	Symbol	Min	Typ	Max	Unit	Note
PSNR						
Spurs from power noise 50mV ripple V_{DD} = 1.8V	PSNR	–	-76	–	dBc	100 kHz sine wave
		–	-75	–	dBc	200 kHz sine wave
		–	-75	–	dBc	500 kHz sine wave
		–	-75	–	dBc	1 MHz sine wave
Spurs from power noise 50mV ripple V_{DD} = 2.5 or 3.3V	PSNR	–	-83	–	dBc	100 kHz sine wave
		–	-83	–	dBc	200 kHz sine wave
		–	-83	–	dBc	500 kHz sine wave
		–	-82	–	dBc	1 MHz sine wave

Table 2.2. Environmental Compliance and Package Information

Parameter	Value
Moisture sensitivity level (MSL)	3

Notes:

For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact aeonsemi.com/contact_us

Table 2.3. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Maximum operating temperature	T_{AMAX}	125	℃
Storage temperature	T_S	-55 - 125	℃
Supply voltage	V_{DD_MAX}	-0.5 - 3.8	V
Input voltage	V_{IN_MAX}	-0.5 - V_{DD}+0.3	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
ESD CDM (JESD22-C101)	CDM	1.0	kV
Solder Temperature[2]	T_{PEAK}	260	℃
Solder time at T_{PEAK}[2]	T_P	20 - 40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

3. Package Outline Drawing

Figure 3.1. shows the package outline drawing for the AS5018 devices. Details of dimension for different size options are listed in Table 3.1.

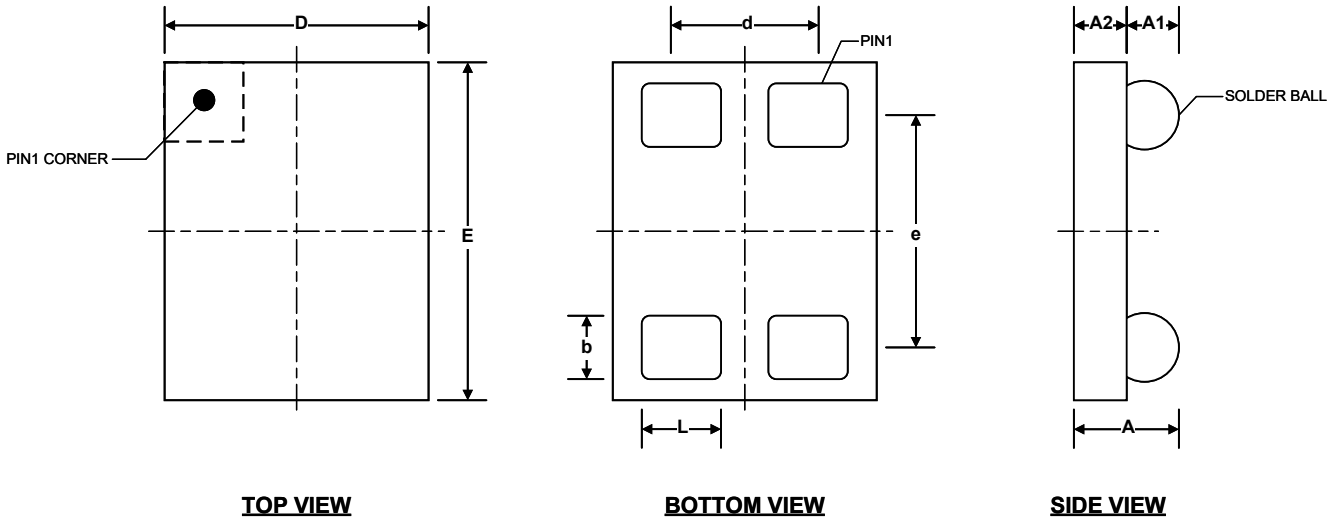


Figure 3.1. Package Outline Drawing

Table 3.1. Dimensions of Package Outline Drawing (um)

Symbol	Min	Nom	Max
A	505	540	575
A1	120	130	140
A2	385	410	435
b	225	235	245
d	–	410 BSC	–
D	1027.2	1052.2	1077.2
d	–	958.2 BSC	–
E	1243.2	1268.2	1293.2
L	250	260	270

4. Recommended PCB Land Pattern

Figure 4.1. shows the drawing of recommended PCB land pattern for the AS5018 devices. Details of dimension for different size options are listed in Table 4.1.

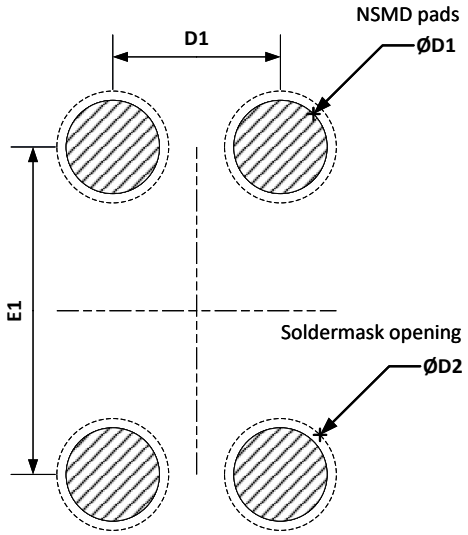


Figure 4.1. Recommended PCB Land Pattern

Table 4.1. Dimensions of Recommended PCB Land Pattern (mm)

Symbol	1210 Package
D1	0.41
ØD1	0.25
ØD2	0.35
E1	1.00

Notes:

The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8 1 for the pads.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5. Top Mark

Figure 5.1. shows the top mark specifications for the AS5018 devices. Description of each line is listed in Table 5.1.

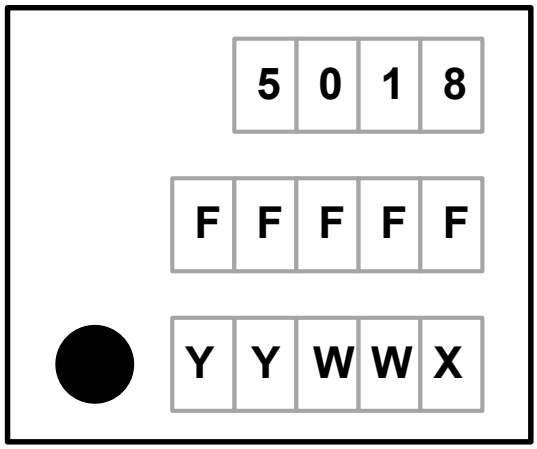


Figure 5.1. Top Mark

Table 5.1. Top Mark Description

Line	Position	Description
1	1-4	Device Name
2	1-5	Unique 5-digit Device Configuration Number
3	1	Pin 1 orientation mark (dot)
	2-3	Year (last two digits of the year), to be assigned by assembly site (ex: 2025 = 25)
	4-5	Calendar Work Week number (1-53), to be assigned by assembly site
	6	Manufacturer code

6. Packing Specification

Figure 6.1. shows the packing specifications for the AS5018 devices. Details of the tape specifications are listed in Table 6.1.
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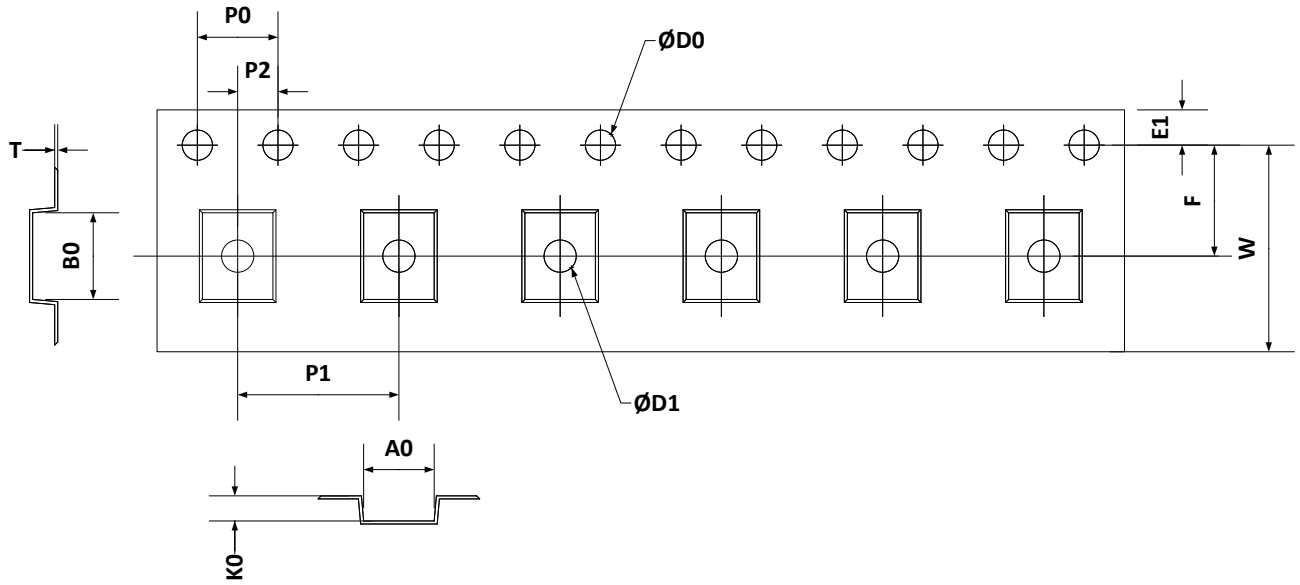

Figure 6.1. Tape Specification

Table 6.1. Dimensions of Tape (mm)

Symbol	1210 Package
A0	1.20 ± 0.03
B0	1.42 ± 0.03
K0	0.63 ± 0.03
E1	1.75 ± 0.10
F	3.50 ± 0.05
W	8.00 (+0.30/-0.10)
T	0.20 ± 0.02
P0	4.00 ± 0.10
P1	4.00 ± 0.10
P2	2.00 ± 0.05
ϕD0	1.55 ± 0.05
ϕD1	0.60 ± 0.05

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8. Revision History

Revision	Date	Description
1.02	Oct 2026	Updated ordering guide
1.01	Oct 2026	Updated several items
0.10	Sep 2025	Corrected several description errors
0.09	Aug 2025	Update the package outline
0.08	May 2024	Correct several mistakes
0.07	Feb 2024	Update the initial tolerance and temperature stability
0.06	Sep 2023	Update the initial tolerance
0.05	Jul 2023	Update the top mark and ordering guide
0.04	Jun 2023	Correct C1AW transaction to C1EAW
0.03	Jun 2023	Add C1 data programming interface protocol
0.02	May 2023	Updated the core power consumption
0.01	Nov 2022	Initial release