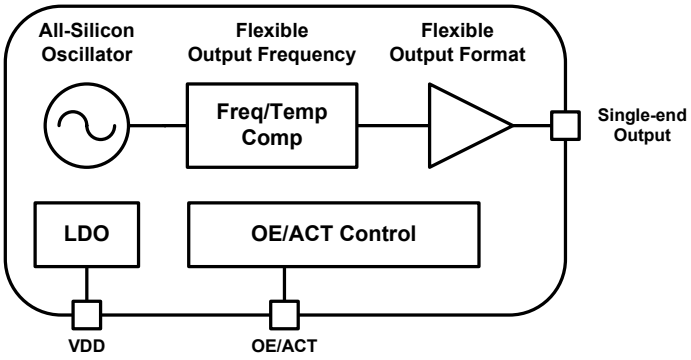
AS511 Low Jitter LVCMOS Silicon Oscillator

Description

The AS511 Arcadium™ all-silicon CMOS oscillator utilizes proprietary frequency synthesis and sensor technologies to provide a quartz-free, MEMS-free, low jitter clock at any output frequency. The device is factory-programmed to a fixed frequency ranging from 10 kHz to 212.5 MHz with 1 Hz resolution and maintains low jitter across its operating range. It uses on-chip temperature and strain sensors, and an advanced LC tank architecture to achieve excellent reliabilities even in high impact shock scenarios.

AS511's on-chip power supply filtering provides industry-leading power supply noise rejection, simplifying the task of generating low jitter clocks in noisy systems that use switched-mode power supplies. Offered in an industry-standard 3225 and 5032 package, the AS511 has a dramatically simplified supply chain that enables Aeonsemi to ship samples shortly after receipt of order. Specific frequency and OE/ACT are factory programmed at time of shipment, eliminating the long lead times associated with custom frequencies. This process also guarantees 100% electrical testing of every device before shipment.



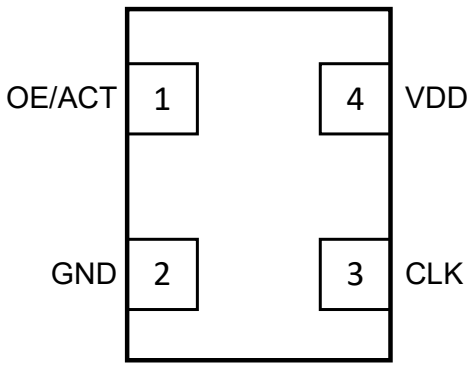
Key Features

- Quartz-free and MEMS-free without mechanical moving parts
- LVCMOS output: 10 kHz to 212.5 MHz
- Low jitter: 350 fs Typ
  (12 kHz – 20 MHz, @156.25 MHz)
- Temperature stability:
  - ±20 ppm (-20 to 85 ℃)
  - ±35 ppm (-40 to 85 ℃)
  - ±35 ppm (-40 to 105 ℃)
- Integrated LDO for on-chip power supply noise filtering
- Support 1.8V, 2.5V, 3.3V V_{DD} supply operation
- Industrial standard 3225 and 5032 package footprints

Application

- 1G/10G/40G/100G/200G Ethernet
- Servers, switches, storage, NICs
- Test and measurement
- Clock and data recovery
- FPGA/ASIC clocking

Pin definition



Top view

Pin#	Description
1	OE = Output enable. Active high ACT = Device active. Active high
2	GND = Ground
3	CLK = Clock output
4	VDD = Power supply

1. Ordering Guide

XO Series	Description
511	Fixed Frequency

	Device Type
A	General
X[1]	Factory defined setting

	Package
A	5032
B	3225

	Temperature Grade
I	-40 to 85 °C
E	-40 to 105 °C

511 A A A - - - - - - - - A B I T

	Frequency Range
A	<= 50 MHz
B	> 50 MHz

	Pin#1
A	OE
C	ACT

Device Revision

Frequency Code[2]	Description
Mxxxxxxx	F_{CLK} < 1 MHz
xMxxxxxx	1 MHz <= F_{CLK} < 10 MHz
xxMxxxxx	10 MHz <= F_{CLK} < 100 MHz
xxxMxxxx	100 MHz <= F_{CLK} <= 212.5 MHz

Code	Packing type	Qty
T	7-inch reel	250
R	13-inch reel	2500
F	13-inch reel	5000
<blank>	Bulk	Sample

Note:

1. “X” refers to the ID for the unique configuration with factory-defined settings, the value ranges from “B” to “Z”.
2. For example: 125 MHz = 125M0000; 33.33333 MHz = 33M33333.

2. Electrical Specifications

Table 2.1. Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating Temperature Range						
Temperature Range	T_A	-40	–	85	℃	Industrial grade
		-40	–	105	℃	Extended industrial grade
Supply Voltage and Power Consumption						
Supply Voltage	V_{DD}	1.62	–	3.63	V	
Supply Current (F_{CLK} = 25 MHz)	I_{DD}	–	40	50	mA	Tristate Hi-Z (OE = 0)
		–	1	2	mA	Ready State (ACT = 0)
		–	40	55	mA	LVCMOS output (C_L=15pF)
Frequency Range						
Frequency Range	F_{CLK}	0.01	–	212.5	MHz	LVCMOS output
Frequency Tolerance						
Initial frequency accuracy	F_{INIT}	-10	–	10	ppm	Inclusive of initial frequency tolerance at 25℃ and variations over supply voltage, load and humidity after soldering-reflow shift settles.
Temperature stability	F_{STAB}	-20	–	20	ppm	-20 to 85℃
		-35	–	35	ppm	-40 to 85℃
		-35	–	35	ppm	-40 to 105℃
Aging	F_{AGING}	-5	–	5	ppm	10 years at 25 ℃
IO Characteristics						
Output enable (OE)	V_{IH}	0.7×V_{DD}	–	–	V	Input high voltage
	V_{IL}	–	–	0.3×V_{DD}	V	Input low voltage
	R_{PUP}	–	50	–	kΩ	Internal pull-up resistor to V_{DD}
	T_D	–	–	3	us	Output disable time, F_{CLK} >10 MHz
	T_E	–	–	20	us	Output enable time, F_{CLK} >10 MHz
Device active (ACT)	V_{IH}	0.7×V_{DD}	–	–	V	Input high voltage
	V_{IL}	–	–	0.3×V_{DD}	V	Input low voltage
	R_{PUP}	–	50	–	kΩ	Internal pull-up resistor to V_{DD}
	T_D	–	–	3	us	Output disable time, F_{CLK} >10 MHz
	T_S	–	–	40	us	Device standby time, F_{CLK} >10 MHz
	T_E	–	–	400	us	Device enable time, F_{CLK} >10 MHz
Output Characteristics						
Powerup time	T_{OSC}	–	–	4	ms	Time from power reaches 0.9 × V_{DD} to output frequency (F_{CLK}) within spec
Duty cycle	DC	45	–	55	%	LVCMOS (C_L=15pF)
Rise/Fall time (20% to 80% VPP)	$T_{R/F}$	–	0.5	1.5	ns	LVCMOS (C_L=15pF)
LVCMOS	V_{OH}	0.83×V_{DD}	–	–	V	C_L=15pF
	V_{OL}	–	–	0.17×V_{DD}	V	

Continued on next page

Parameter	Symbol	Min	Typ	Max	Unit	Note
Phase Noise and Jitter						
RMS jitter	R_J	–	350	750	fs	F_{CLK} >= 100 MHz
BW: 12 kHz to 20 MHz		–	450	750	fs	F_{CLK} >= 25 MHz
Phase noise	PN_{1k}	–	-83	–	dBc/Hz	Phase noise at 1 kHz offset
125 MHz LVCMOS output	PN_{10k}	–	-111	–	dBc/Hz	Phase noise at 10 kHz offset
V_{DD} = 1.8 to 3.3 V	PN_{100k}	–	-134	–	dBc/Hz	Phase noise at 100 kHz offset
	PN_{1M}	–	-150	–	dBc/Hz	Phase noise at 1 MHz offset
	PN_{10M}	–	-159	–	dBc/Hz	Phase noise at 10 MHz offset
Power Supply Ripple Rejection (PSRR)						
Spurs from power noise	PSRR	–	-76	–	dBc	100 kHz sine wave
50 mV ripple		–	-75	–	dBc	200 kHz sine wave
V_{DD} = 1.8 V		–	-75	–	dBc	500 kHz sine wave
		–	-75	–	dBc	1 MHz sine wave
Spurs from power noise	PSRR	–	-83	–	dBc	100 kHz sine wave
50 mV ripple		–	-83	–	dBc	200 kHz sine wave
V_{DD} = 2.5 or 3.3 V		–	-83	–	dBc	500 kHz sine wave
		–	-82	–	dBc	1 MHz sine wave

Table 2.2. Environmental Compliance and Package Information

Parameter	Value
Moisture sensitivity level (MSL)	1

Notes:

For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact aeonsemi.com/contact_us

Table 2.3. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Maximum operating temperature	T_{AMAX}	125	℃
Storage temperature	T_S	-55 - 125	℃
Supply voltage	V_{DD_MAX}	-0.5 - 3.8	V
Input voltage	V_{IN_MAX}	-0.5 - V_{DD}+0.3	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
ESD CDM (JESD22-C101)	CDM	1.0	kV
Solder Temperature[2]	T_{PEAK}	260	℃
Solder time at T_{PEAK}[2]	T_P	20 - 40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. The device is compliant with JEDEC J-STD-020.

3. Package Outline Drawing

Figure 3.1. shows the package outline drawing for the AS511 devices. Details of dimensions for different size options are listed in Table 3.1. .

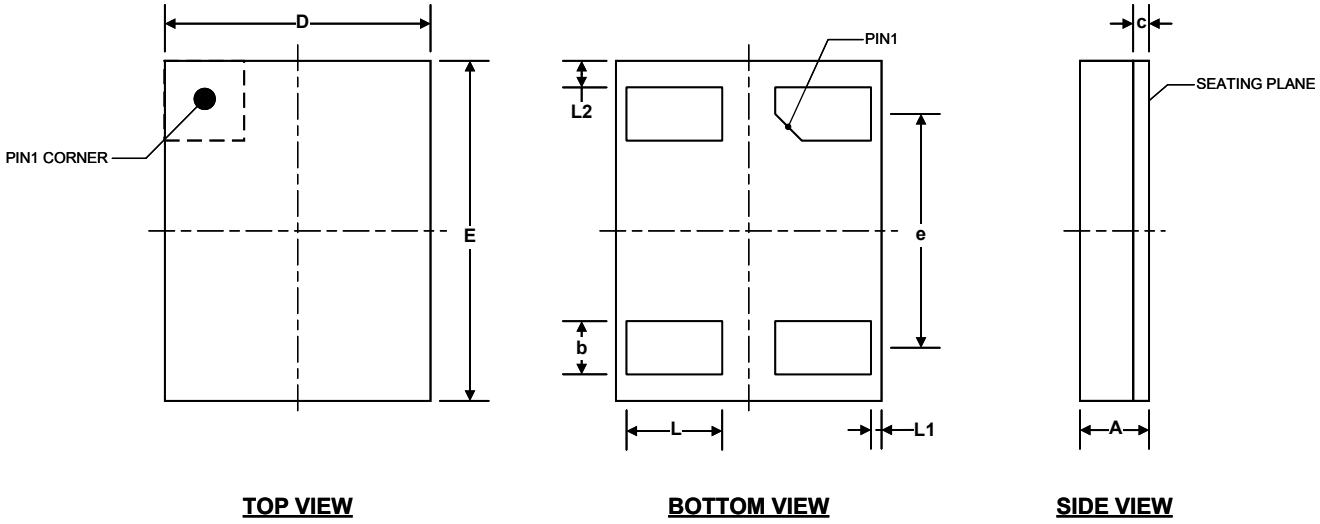


Figure 3.1. Package Outline Drawing

Table 3.1. Dimensions of Package Outline Drawing (mm)

Symbol	5032 Package	3225 Package
A	0.85 ± 0.05	0.85 ± 0.05
b	0.64 ± 0.05	0.90 ± 0.05
D	3.20 ± 0.10	2.50 ± 0.10
e	2.54 BSC	2.10 BSC
E	4.00 ± 0.10	3.20 ± 0.10
L	0.94 ± 0.05	0.70 ± 0.05
L1	0.10 ± 0.05	0.10 ± 0.05

4. Recommended PCB Land Pattern

Figure 4.1. shows the recommended PCB land pattern for the AS511 devices. Details of dimensions for different size options are listed in Table 4.1. .

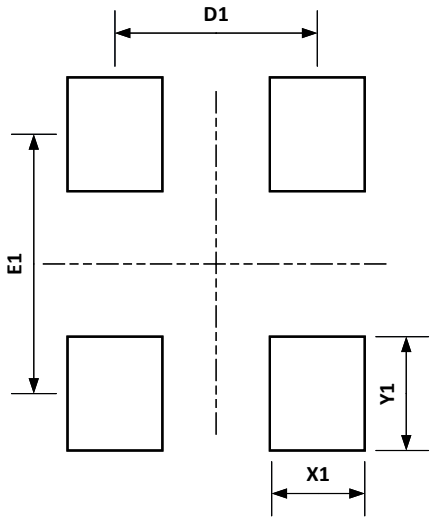


Figure 4.1. Recommended PCB Land Pattern

Table 4.1. Dimensions of Recommended PCB Land Pattern (mm)

Symbol	5032 Package	3225 Package
D1	2.16	1.70
E1	2.54	2.10
X1	1.24	1.00
Y1	0.84	1.10

Notes:

The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 um minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8 1 for the pads.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5. Top Mark

Figure 5.1. shows the top mark specifications for the AS511 devices. Description of each line is listed in Table 5.1.

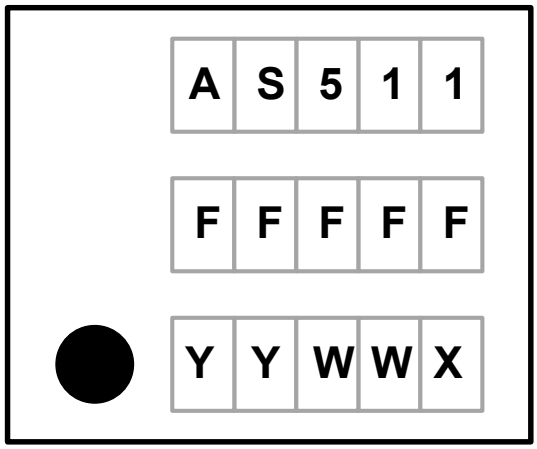


Figure 5.1. Top Mark

Table 5.1. Top Mark Description

Line	Position	Description
1	1-5	Device Name
2	1-5	Unique 5-digit Device Configuration Number
3	1	Pin 1 orientation mark (dot)
	2-3	Year (last two digits of the year), to be assigned by assembly site (ex: 2025 = 25)
	4-5	Calendar Work Week number (1-53), to be assigned by assembly site
	6	Manufacturer code

6. Packing Specification

Figure 6.1. shows the packing specifications for the AS511 devices. Details of the tape specifications are listed in Table 6.1. .

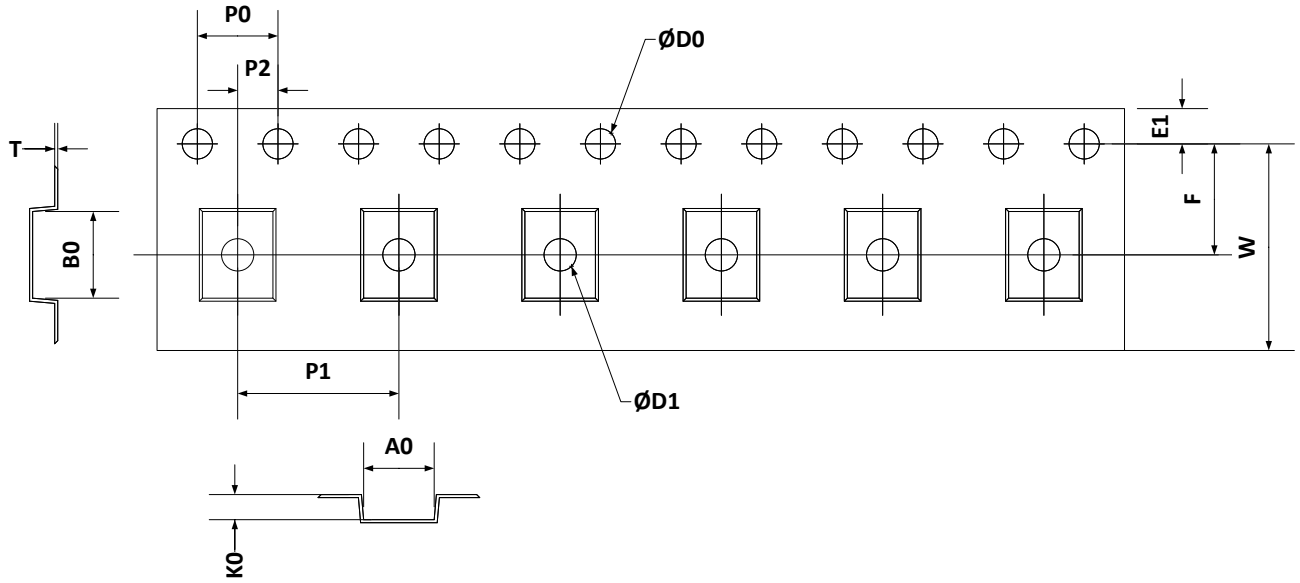


Figure 6.1. Tape Specification

Table 6.1. Dimensions of Tape (mm)

Symbol	5032 Package	3225 Package
A0	3.50 ± 0.10	2.80 ± 0.10
B0	4.30 ± 0.10	3.50 ± 0.10
K0	1.25 ± 0.10	1.05 ± 0.10
E1	1.75 ± 0.10	1.75 ± 0.10
F	5.50 ± 0.05	5.50 ± 0.05
W	12.00 ± 0.30	12.00 ± 0.30
T	0.30 ± 0.05	0.30 ± 0.05
P0	4.00 ± 0.10	4.00 ± 0.10
P1	8.00 ± 0.10	8.00 ± 0.10
P2	2.00 ± 0.05	2.00 ± 0.05
ϕD0	1.50 ± 0.10	1.50 ± 0.10
ϕD1	1.60 ± 0.10	1.60 ± 0.10

7. Important Notice and Disclaimer

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8. Revision History

Revision	Date	Description
1.16	Oct 2026	Updated ordering guide
1.15	Aug 2026	Removed paragraph first-line indentation Corrected top mark position table
1.13	Aug 2025	Corrected the tape specification
1.12	Aug 2024	Add packing specification
1.11	Mar 2024	Updated the frequency offset
1.10	Jul 2022	Updated the top mark specification
1.01	Dec 2021	Adjusted the PCB land pattern dimensions
1.00	Sep 2021	With certain specification update
0.95	Jun 2021	Corrected the Ordering Guide Insert -40 to 105 ℃ temperature range option Insert section “Important Notice and Disclaimer”
0.20	Mar 2021	Changed the frequency range and ordering guide
0.10	Feb 2021	Initial release