AS5224 Ultra Low Jitter Low Power Differential VCTCXO

Description

The AS5224 is a voltage-controlled temperature-compensated crystal oscillator (VCTCXO) that provides low-amplitude differential output clocks from 10 MHz to 156.25 MHz. Digital temperature sensing and frequency compensation maintain a stable reference clock, while the voltage-control input enables smooth frequency adjustment around the factory-programmed nominal frequency.

The tuning slope is programmable for the required application, with a maximum slope of 6 ppm/V. The center control voltage and frequency pull range are factory configured through the device ordering code. The AS5224 operates from a wide 1.8 V to 3.3 V supply range, and its on-chip LDO provides robust power supply noise rejection, simplifying external supply filtering.

The AS5224 supports configurable output amplitude from 0.8V to 1.2V. The 0.8V output option is compliant with clipped sine (0.8V CS) which is widely adopted in the industry. The two outputs can be configured as in-phase or complementary. When it's configured as complementary, the outputs can be used as a differential pair.

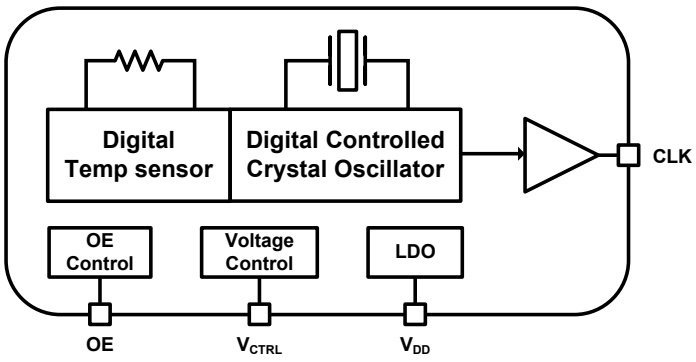
The AS5224 is available in the industry-standard 2016 package with industrial, extended industrial, and automotive device grades. Its wide operating range, low-jitter output, and programmable voltage control support precision timing in microwave backhaul, communication networks, data center interconnects, AI server clusters, and high-speed optical modules.

Key Features

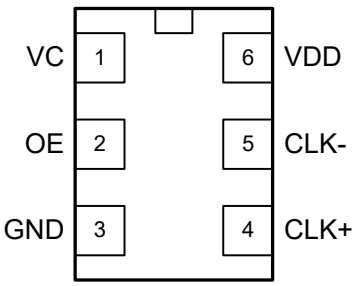
- Frequency range: 10 to 156.25 MHz
- Dual LVCMOS and low-amplitude differential output options
- 0.8, 1.0, 1.2V output amplitude/swing options
- Ultra-low jitter: 52 fs Typ
  (12 kHz – 20 MHz, @156.25 MHz)
- Ultla-low core power: 5mA
- Operating temperature range:
  - -40 to 85 ℃ (Industial grade)
  - -40 to 105 ℃ (Extended-Industial grade)
  - -40 to 105 ℃ (AEC-Q100 grade 2)
- Temperature stability:
  - ±5 ppm (Grade S)
  - ±20 ppm (Grade D)
- Programmable tuning slope up to 6 ppm/V
- Integrated LDO for on-chip power supply noise filtering
- Support 1.8V, 2.5V, 3.3V V_{DD} supply operation
- Standard DFN 2016 package

Application

- Microwave backhaul
- Communication networks
- Data center interconnect
- AI server clusters
- Smart network interface card
- High-speed optical module



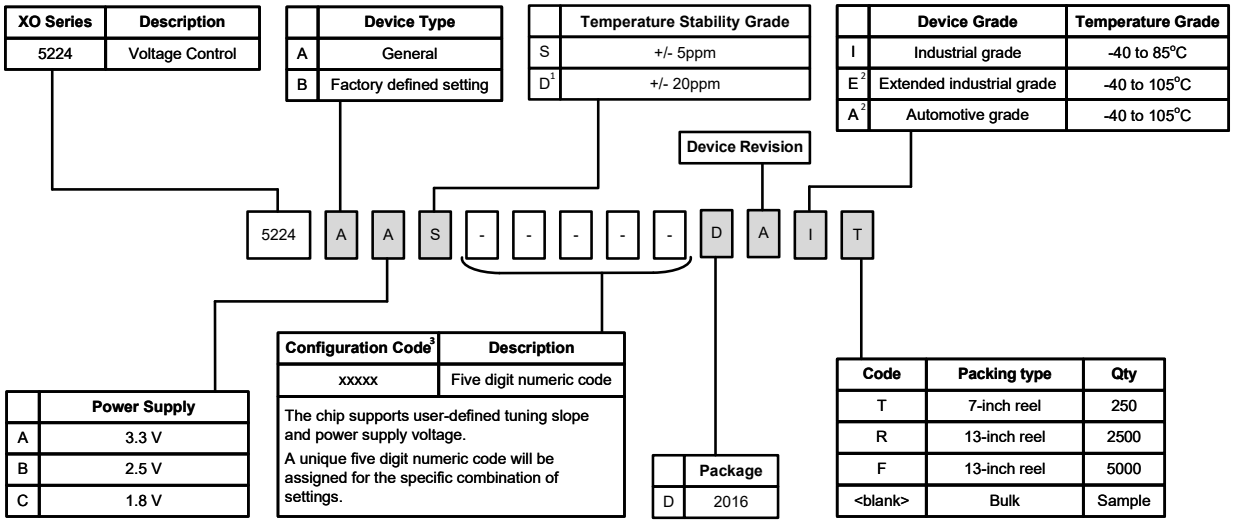
Pin definition



Top view

Pin#	Description
1	VC = Voltage control input
2	OE = Output enable. Active high
3	GND = Ground
4	CLK+ = Clock output
5	CLK- = Complementary clock output
6	VDD = Power supply

1. Ordering Guide



Note:

1. Temperature compensation is not applied for grade-D device. Frequency is calibrated at 25 ℃ in production test.
2. Contact Aeonsemi for extended-industrial and automotive-grade devices.
3. The five-digit numeric code is an identification of the configurations. Check the datasheet appendix for the details.

2. Electrical Specifications

Table 2.1. Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating Temperature Range						
Temperature Range	T_A	-40	–	85	℃	Industrial grade
		-40	–	105	℃	Extended industrial grade
		-40	–	105	℃	Automotive AEC-Q100 Grade2
Supply Voltage and Power Consumption						
Supply Voltage	V_{DD}	1.62	–	3.63	V	Core voltage
Driver Regulator Voltage	V_R	0.8	–	1.2	V	Regulator voltage
Supply Current	I_{CORE}	–	4	5	mA	Tristate Hi-Z (Output disabled)
(F_{CLK} = 156.25 MHz)	I_{DRV}	–	1.6	2	mA	0.8V LVCMOS (Load=10pF//10kΩ)
		–	2	2.5	mA	1.0V LVCMOS (Load=10pF//10kΩ)
		–	2.4	3	mA	1.2V LVCMOS (Load=10pF//10kΩ)
		–	6	7	mA	0.8V Differential (100 Ω termination)
		–	7.5	9	mA	1.0V Differential (100 Ω termination)
		–	9	11	mA	1.2V Differential (100 Ω termination)
Frequency Range						
Frequency Range	F_{CLK}	10	–	156.25	MHz	Standard frequency options Contact Aeonsemi for other frequency options
		10, 16, 19.2, 20, 25, 26, 32, 38.4, 50, 52, 100, 155.52, 156.25				
Frequency Tolerance						
Initial frequency accuracy[1]	F_{INIT}	-2	–	2	ppm	Grade S
		-5	–	5	ppm	Grade D
Temperature stability over full temp range[2]	F_{STAB}	-5	–	5	ppm	Grade S
		-20	–	20	ppm	Grade D
Aging	S_{AGING}	-1	–	1	ppm/y	Maximum aging slope at 25 ℃
	F_{AGING}	-3	–	3	ppm	10-year aging at 25℃
Notes: 1. Inclusive of initial frequency tolerance at 25℃, variations over supply voltage, load and humidity after 2 times of reflows. 2. Frequency / temperature characteristics with offset removed.						
VCXO Control Characteristics						
Control voltage input	V_C	0	–	V_{DD}	V	Input reference voltage range
Center control voltage[3]	V_{CEN}	–	$V_{DD}/2$	–	V	Factory-programmable center voltage
Tuning slope[3]	K_V	–	–	6	ppm/V	Factory-programmable tuning slope
Control voltage linearity	Lin	-3	–	3	%	Linearity error
Notes: 3. The center control voltage and tuning slope are factory-programmable to meet application-specific requirements. Contact aeonsemi.com/contact_us to obtain the unique part number for the required configuration.						

Continued on next page

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output Characteristics						
Powerup time	T_{OSC}	–	–	4	ms	Time from power reaches 0.9 × V_{DD} to output frequency (F_{CLK}) within spec
Duty cycle	DC	45	–	55	%	All formats
Rise/Fall time	$T_{R/F}$	–	0.5	1.5	ns	LVCMOS (Load=10pF//10kΩ)
(20% to 80% VPP)		–	–	350	ps	Differential (100 Ω termination)
0.8V differential	V_{OC}	0.15	0.20	0.25	V	Mid-level
	V_O	0.70	0.80	0.90	V_{PP}	Swing (Diff)
1.0V differential	V_{OC}	0.20	0.25	0.30	V	Mid-level
	V_O	0.90	1.00	1.10	V_{PP}	Swing (Diff)
1.2V differential	V_{OC}	0.25	0.30	0.35	V	Mid-level
	V_O	1.10	1.20	1.30	V_{PP}	Swing (Diff)
LVCMOS	V_{OH}	0.83×V_R	–	–	V	LVCMOS (Load=10pF//10kΩ)
	V_{OL}	–	–	0.17×V_R	V	
Phase Noise and Jitter						
RMS jitter	R_J	–	52	70	fs	F_{CLK} >= 100 MHz
BW: 12k - 20MHz		–	100	200	fs	F_{CLK} >= 50 MHz
		–	150	300	fs	F_{CLK} <50 MHz
Phase noise	PN_{1k}	–	-137	–	dBc/Hz	Phase noise at 1kHz offset
156.25MHz 0.8V	PN_{10k}	–	-148	–	dBc/Hz	Phase noise at 10kHz offset
differential output	PN_{100k}	–	-155	–	dBc/Hz	Phase noise at 100kHz offset
V_{DD} = 1.8 - 3.3V	PN_{1M}	–	-162	–	dBc/Hz	Phase noise at 1MHz offset
	PN_{10M}	–	-163	–	dBc/Hz	Phase noise at 10MHz offset
PSNR						
Spurs from power noise	PSNR	–	-76	–	dBc	100 kHz sine wave
50mV ripple		–	-75	–	dBc	200 kHz sine wave
V_{DD} = 1.8V		–	-75	–	dBc	500 kHz sine wave
		–	-75	–	dBc	1 MHz sine wave
Spurs from power noise	PSNR	–	-83	–	dBc	100 kHz sine wave
50mV ripple		–	-83	–	dBc	200 kHz sine wave
V_{DD} = 2.5 or 3.3V		–	-83	–	dBc	500 kHz sine wave
		–	-82	–	dBc	1 MHz sine wave

Table 2.2. Environmental Compliance and Package Information

Parameter	Value
Moisture sensitivity level (MSL)	3

Notes:

For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact aeonsemi.com/contact_us

Table 2.3. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Maximum operating temperature	T_{AMAX}	125	℃
Storage temperature	T_S	-55 - 125	℃
Supply voltage	V_{DD_MAX}	-0.5 - 3.8	V
Input voltage	V_{IN_MAX}	-0.5 - V_{DD}+0.3	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
ESD CDM (JESD22-C101)	CDM	1.0	kV
Solder Temperature[2]	T_{PEAK}	260	℃
Solder time at T_{PEAK}[2]	T_P	20 - 40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

3. Recommended Output Terminations

3.1. Differential Output

The output drivers support AC-coupled or DC-coupled terminations as shown in figures below.

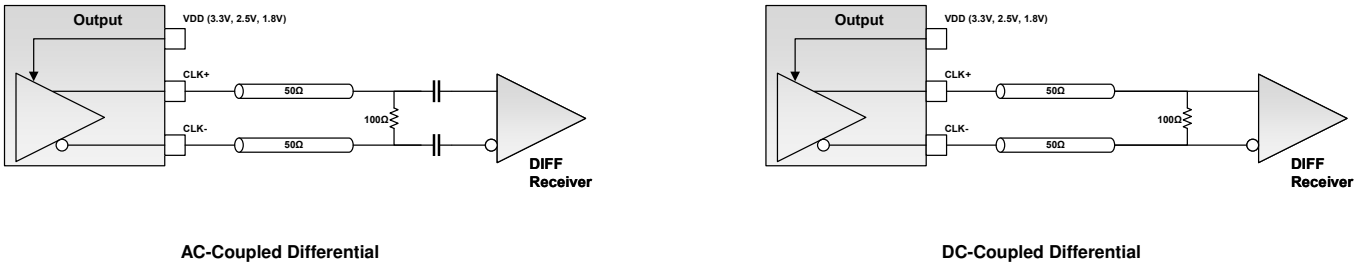


Figure 3.1. Differential Output Terminations

3.2. CMOS Output

Dual CMOS output format options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple XOs with a single AS5224 device.

Figure 3.2. Integrated 1:2 CMOS Buffer Supports In-Phase or Complementary Outputs

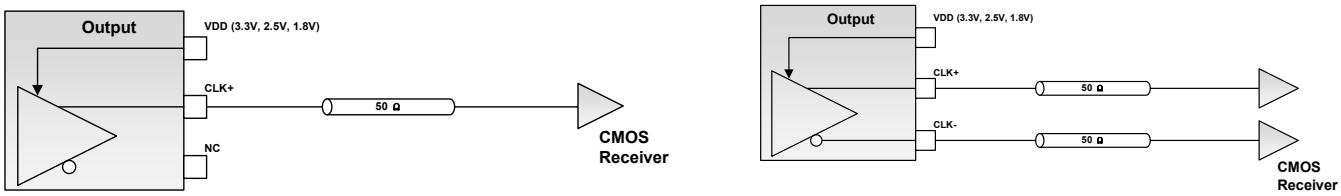


Figure 3.3. LVCMOS Output Terminations

4. Package Outline Drawing

Figure 4.1. shows the package outline drawing for the AS5224 devices. Details of dimension for different size options are listed in Table 4.1.

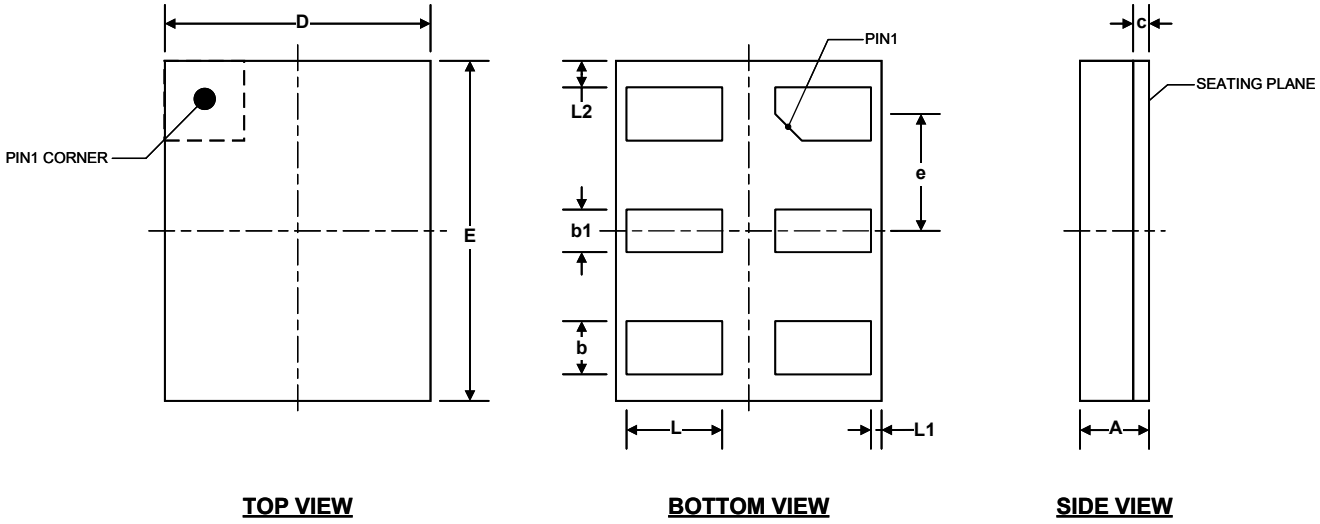


Figure 4.1. Package Outline Drawing

Table 4.1. Dimensions of Package Outline Drawing (mm)

Symbol	Min	Nom	Max
A	0.790	0.890	0.990
b	0.225	0.300	0.375
b1	0.225	0.300	0.375
D	1.550	1.600	1.650
e	–	0.750 BSC	–
E	1.950	2.000	2.050
L	0.375	0.450	0.525
L1	0.025	0.100	0.175

5. Recommended PCB Land Pattern

Figure 5.1. shows the drawing of recommended PCB land pattern for the AS5224 devices. Details of dimension for different size options are listed in Table 5.1.

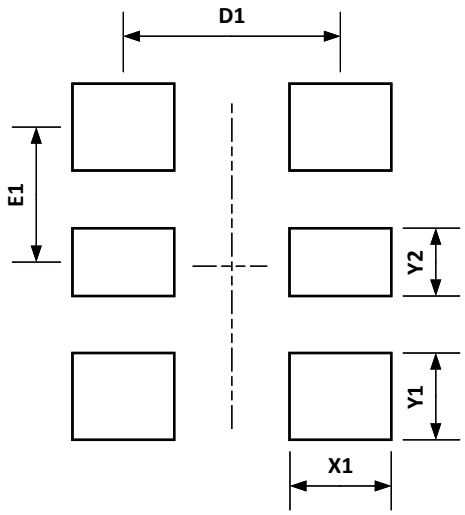


Figure 5.1. Recommended PCB Land Pattern

Table 5.1. Dimensions of Recommended PCB Land Pattern (mm)

Symbol	2016 Package
D1	1.05
E1	0.75
X1	0.75
Y1	0.50
Y2	0.50

Notes:

The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8 1 for the pads.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6. Top Mark

Figure 6.1. shows the top mark specifications for the AS5224 devices. Description of each line is listed in Table 6.1.

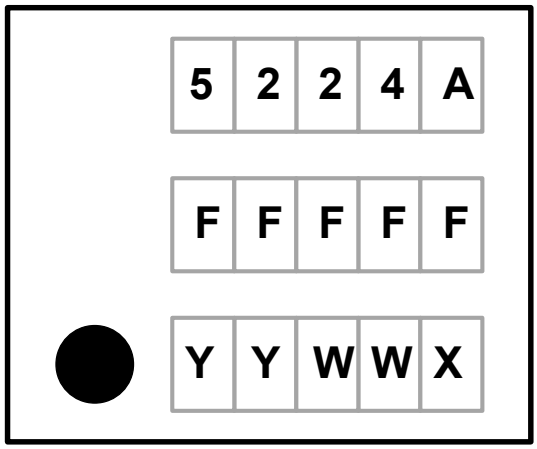


Figure 6.1. Top Mark

Table 6.1. Top Mark Description

Line	Position	Description
1	1-5	Device Name
2	1-5	Unique 5-digit Device Configuration Number
3	1	Pin 1 orientation mark (dot)
	2-3	Year (last two digits of the year), to be assigned by assembly site (ex: 2025 = 25)
	4-5	Calendar Work Week number (1-53), to be assigned by assembly site
	6	Manufacturer code

7. Packing Specification

Figure 7.1. shows the packing specifications for the AS5224 devices. Details of the tape specifications are listed in Table 7.1.
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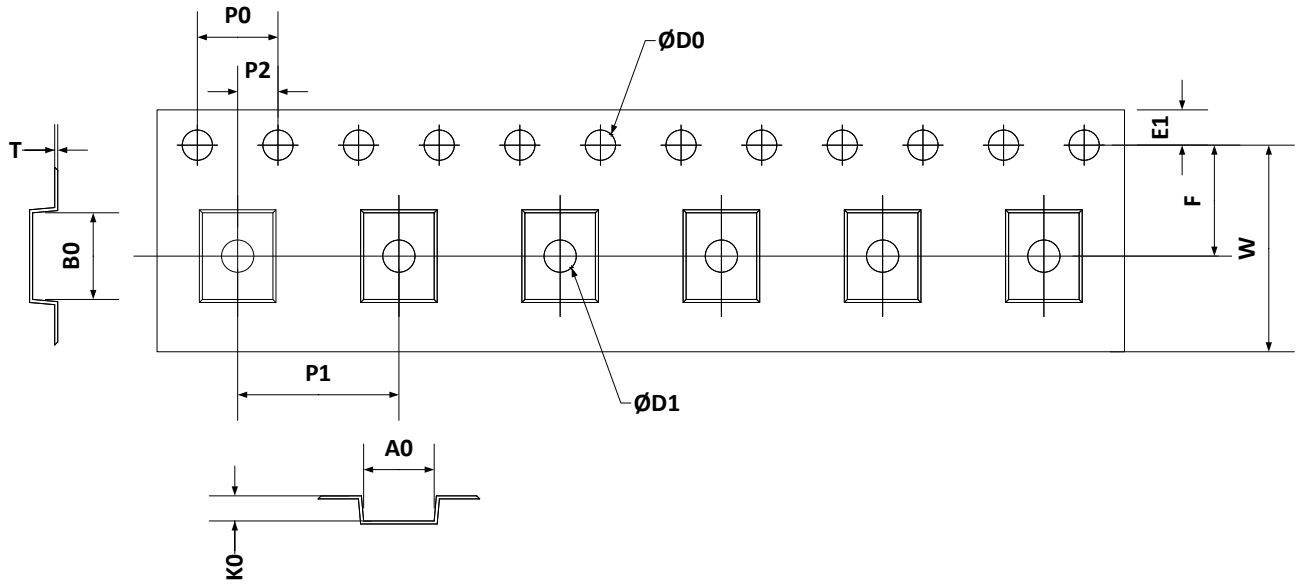

Figure 7.1. Tape Specification

Table 7.1. Dimensions of Tape (mm)

Symbol	2016 Package
A0	1.96 ± 0.05
B0	2.36 ± 0.05
K0	1.20 ± 0.05
E1	1.75 ± 0.10
F	3.50 ± 0.05
W	8.00 ± 0.10
T	0.25 ± 0.05
P0	4.00 ± 0.10
P1	4.00 ± 0.10
P2	2.00 ± 0.05
ϕD0	1.50 (+0.10/-0)
ϕD1	1.05 ± 0.10

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9. Revision History

Revision	Date	Description
1.06	Oct 2026	Updated ordering guide
1.05	Aug 2026	Removed paragraph first-line indentation Corrected top mark position table
1.03	Mar 2026	Updated the Top Mark Rule
1.02	Sep 2025	Corrected several description errors
1.01	Aug 2025	Officially release as mass production version
0.09	Feb 2025	Added ”2016” package outline diagram
0.08	Aug 2024	Updated several items
0.07	Apr 2024	Remove the package outline drawings temporarily
0.06	Feb 2024	Updated the ”Ordering guide”
0.05	Aug 2023	Revised the stability for D-grade option
0.04	Jul 2023	Updated the package outline
0.03	Jun 2023	Updated the ”Ordering guide” and added phase noise jitter for clock >=100 MHz
0.02	Feb 2023	Updated the ”Temperature Stability Grade” D grade
0.01	Nov 2021	Preliminary release